

FIGURE 1

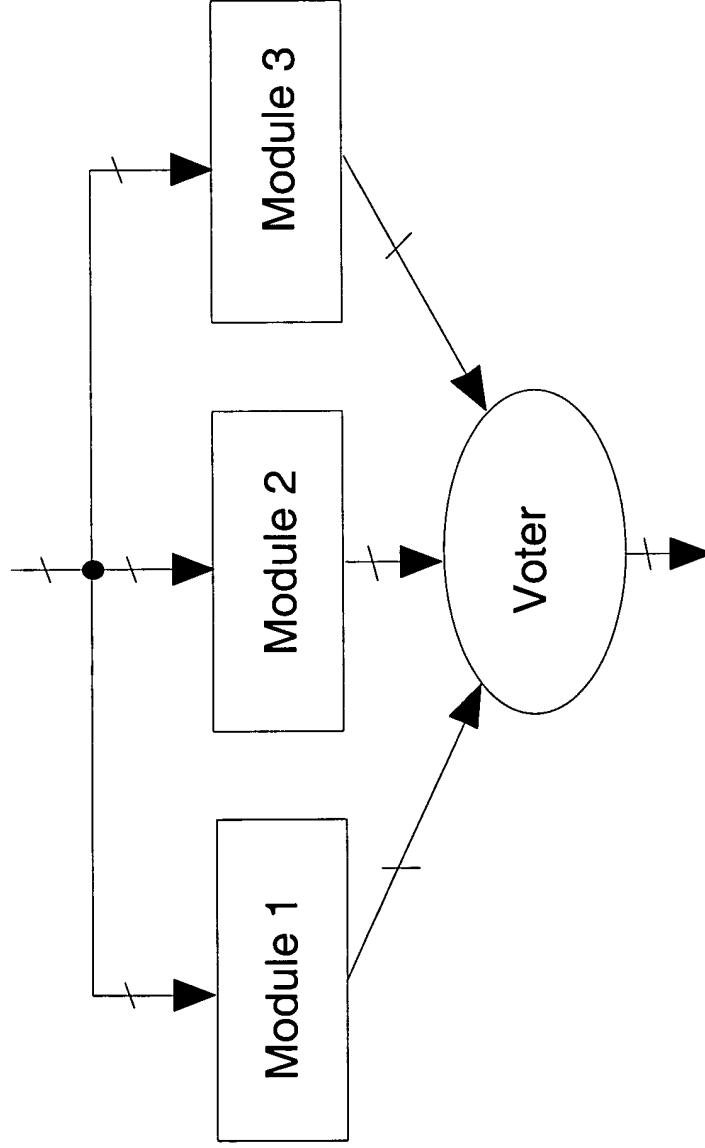


Figure 2 is a block diagram of a logic circuit. The circuit has three inputs:  $Z_1^1$ ,  $Z_1^2$ , and  $Z_1^3$ . The inputs  $Z_1^1$  and  $Z_1^2$  are connected to three AND gates. The input  $Z_1^3$  is connected to the first AND gate. The outputs of the three AND gates are connected to a single OR gate. The output of the OR gate is labeled  $Z_1$ .

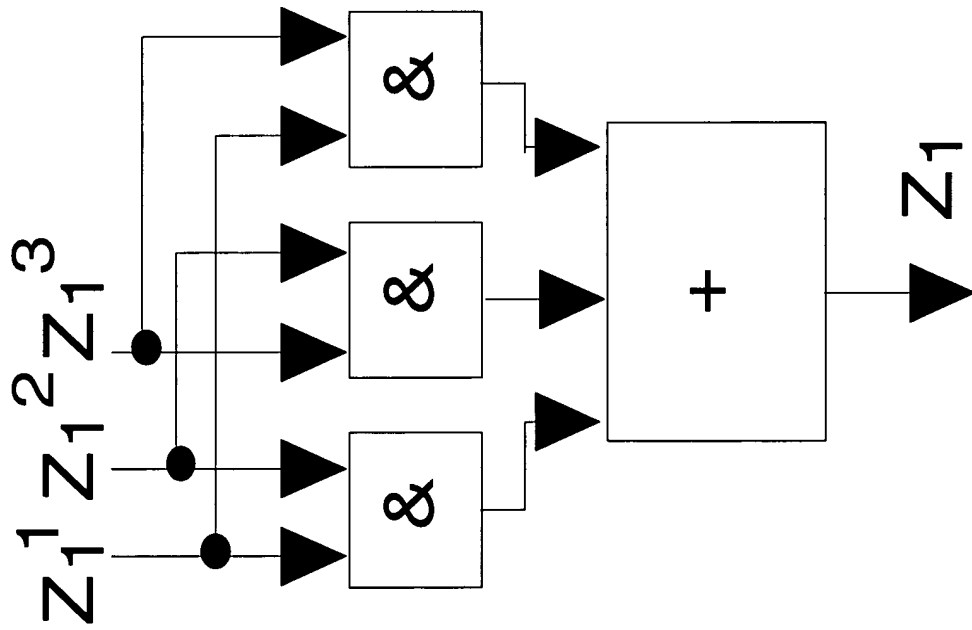
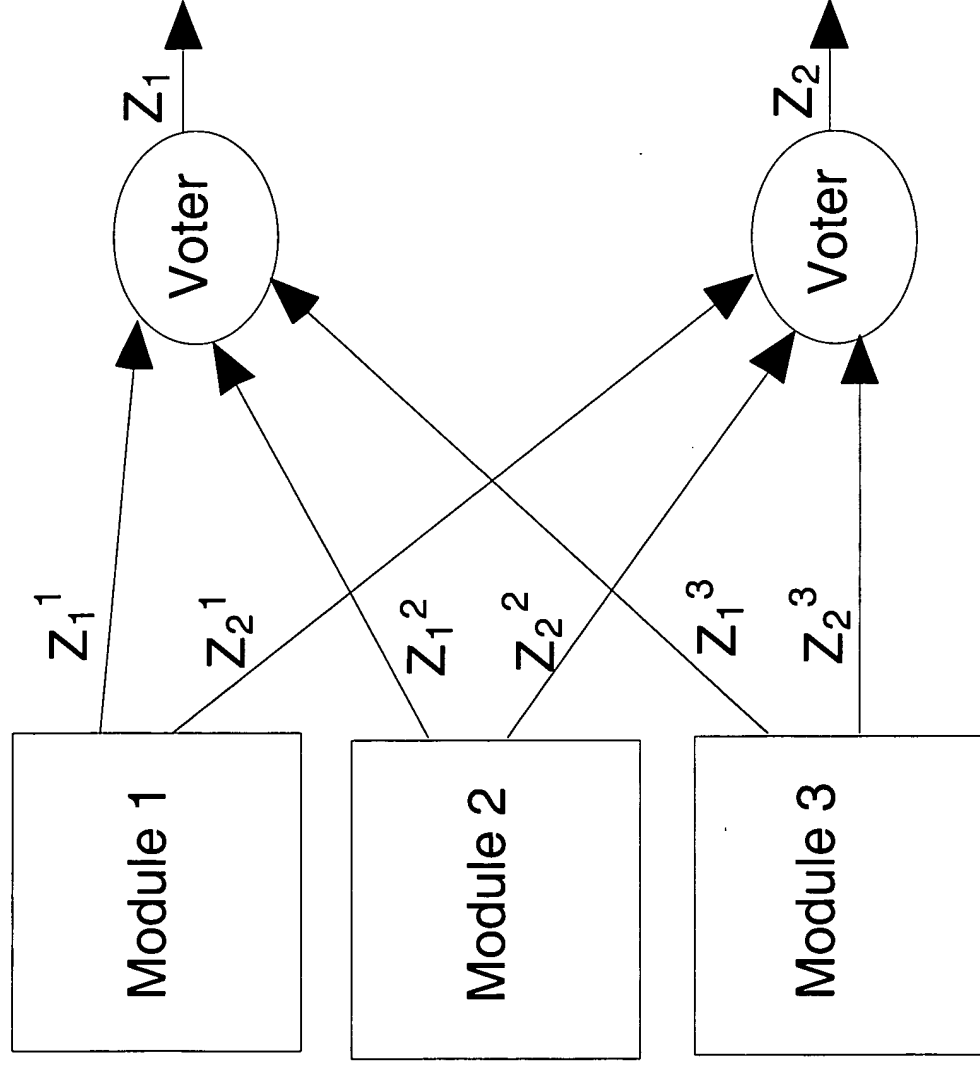


FIGURE 2

FIGURE 3



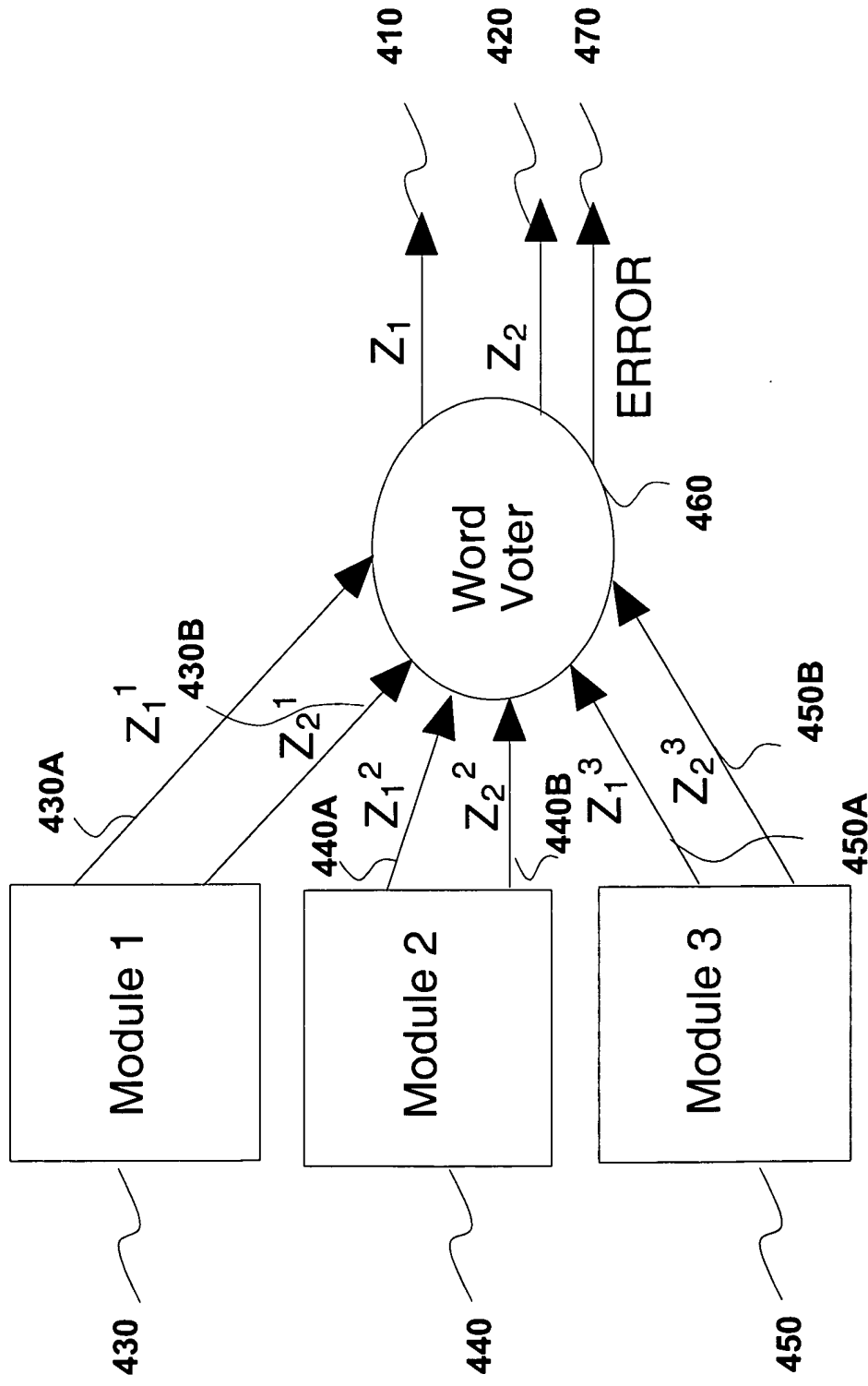


FIGURE 5

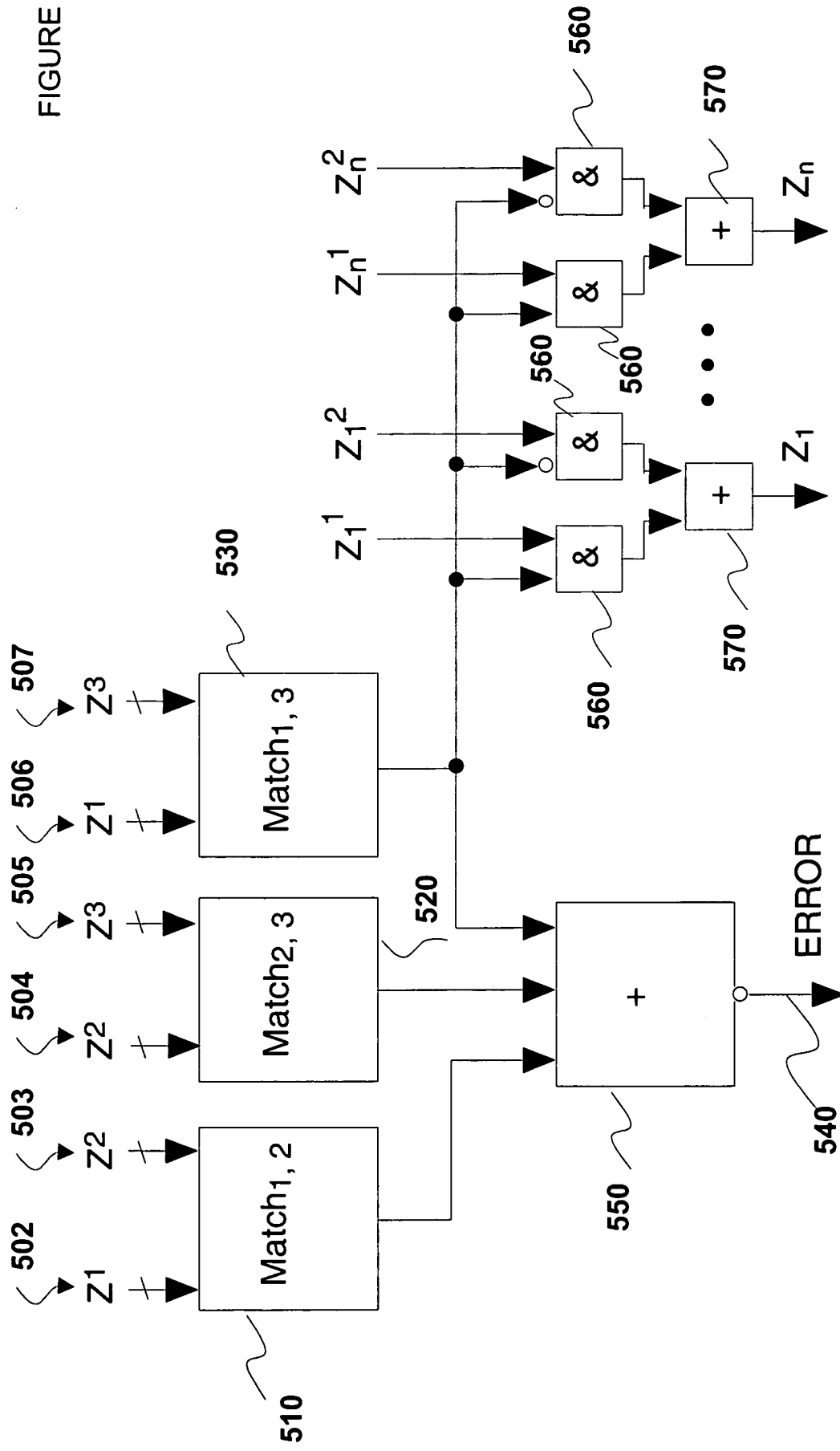


FIG. 6 is a block diagram of a match circuit 600. The match circuit 600 includes a plurality of XOR gates 620 and an AND gate 560. The match circuit 600 is configured to receive a first set of inputs  $Z_1^i, Z_1^j, \dots, Z_n^i, Z_n^j$  and produce a match output  $Match_{i,j}$ . The match circuit 600 is also labeled with reference numerals 600, 610, 560, 620, and 620.

FIGURE 6

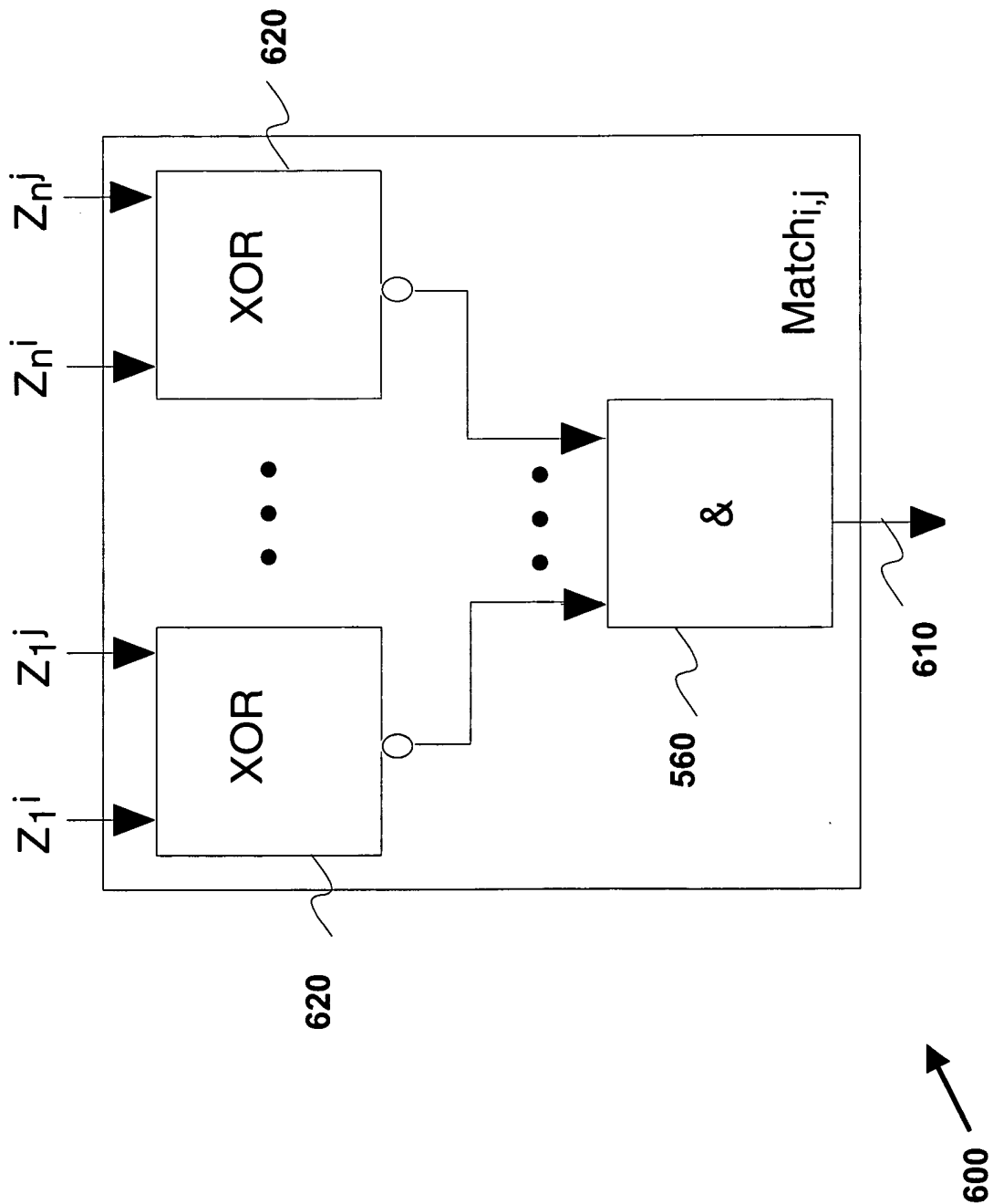


FIGURE 7

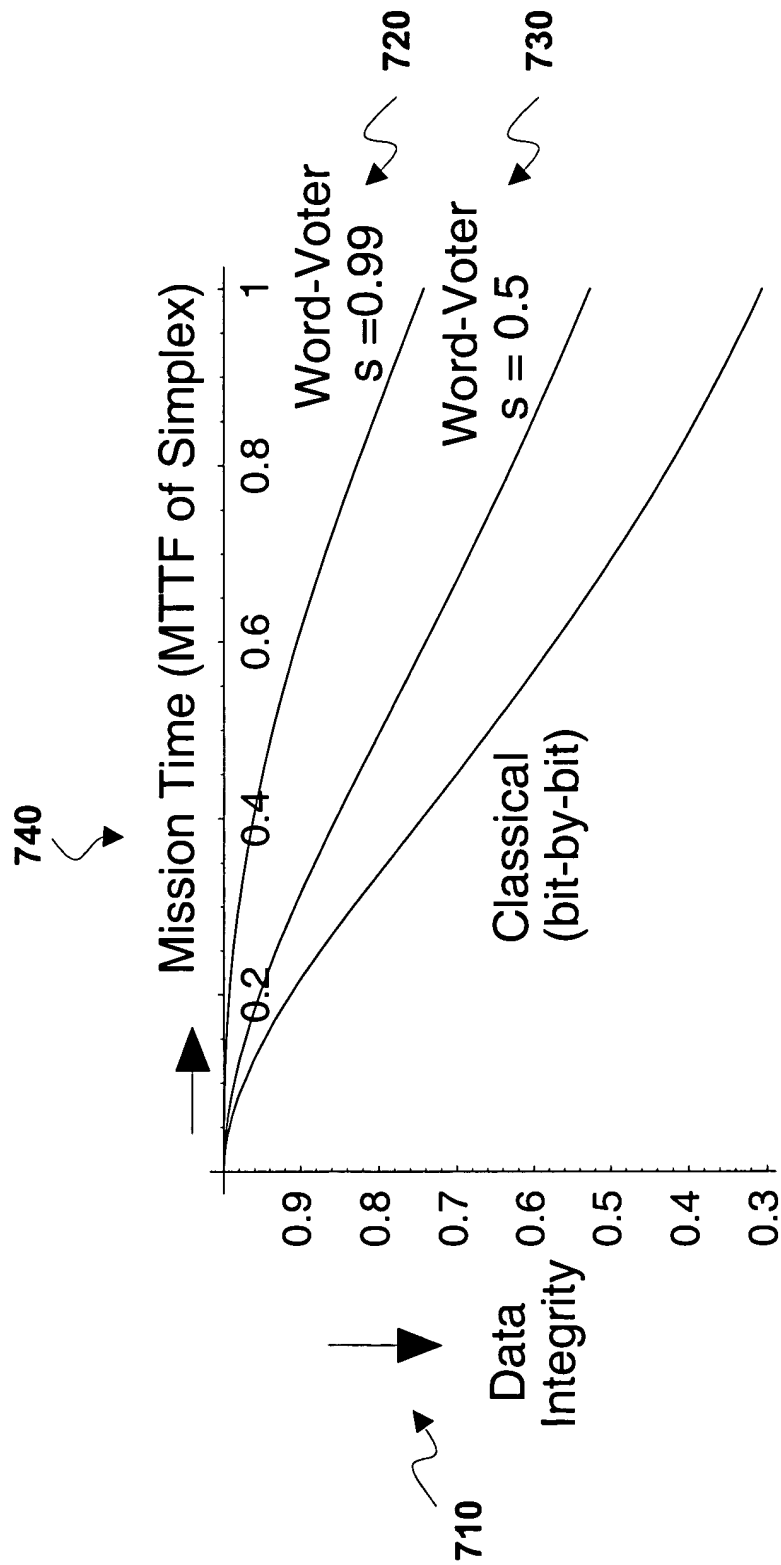


FIGURE 8

